DECchip 21041
PCI Ethernet LAN Controller

Data Sheet

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1 DECchip 21041 Overview

The DECchip 21041 PCI Ethernet LAN Controller (21041) provides a direct interface connection to the peripheral component interconnect (PCI) bus and adapts easily to most other standard buses. The 21041 provides a direct Ethernet connection to the twisted-pair (TP) interface and attachment unit interface (AUI).

The 21041 operates in two modes: mode 0 and mode 1. In mode 0 operation, the 21041 is software compatible with the DECchip 21040 and functions as a DECchip 21040. In mode 1 operation, the 21041 incorporates enhanced features that are described in this document. For a description of mode 0 operation, refer to the *DECchip 21040 Ethernet LAN Controller for PCI Data Sheet* and the *DECchip 21040 Ethernet LAN Controller for PCI Hardware Reference Manual*.

1.1 General Description

The 21041 interfaces with the PCI using onchip control and status registers (CSRs), and a shared system memory area that is set up mainly during initialization. This minimizes the CPU involvement in the 21041 operation during normal reception and transmission. The 21041 is compliant with the *PCI Local Bus Specification, Revision 2.0*. Bus traffic is also minimized by filtering out received runt frames and by automatically retransmitting collided frames without needing to repeat a fetch from system memory.

The 21041 provides a direct interface to a 64K-, 128K-, or 256K-byte boot ROM. It supports both PCI 3.3-volt and 5.0-volt signaling environments and a power-down mode for energy conservation.

On the network side, the 21041 provides an AUI and a TP interface, enabling a low chip count connection to the two most popular Ethernet interfaces. The 21041 can sustain transmission or reception of minimal-sized, back-to-back packets at full line speed with an interpacket gap (IPG) of 9.6 microseconds. It is also capable of functioning in a full-duplex environment, and it supports IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex network environments.

1.2 Microarchitecture

The following list describes the 21041 microarchitecture components, and Figure 1 shows the microarchitecture.

- PCI interface—Includes all interface functions to the PCI bus; handles all interconnect control signals; executes PCI direct memory access (DMA) and I/O transactions.
- DMA—Contains dual receive and transmit controller; supports programmable burst sizes of up to 32 longwords; handles data transfers between system memory and onchip memory.
- FIFOs—Contains dual 256-byte FIFOs for receive and transmit; supports automatic receive packet deletion (for example, runt packets or after a collision) and packet retransmission after a collision on transmit.
- TxM—Handles all CSMA/CD[1] MAC[2]-level transmit operations and transfers data from transmit FIFO to the serial interface attachment (SIA) for transmission.
- RxM—Handles all CSMA/CD receive operations and transfers the data from the SIA to the receive FIFO.
- SIA—Performs physical layer operations; implements the AUI and 10BASE-T functions, including the Manchester encoder and decoder functions.
- Boot ROM—Includes the required interface to the boot ROM for read and write operations. Accesses to bytes or to longwords (32-bit) are supported.
- SROM—Provides all interface logic to allow accesses to the external serial ROM.
- LEDs—Contains the logic to detect seven network events and to drive them outside the device for LED display. Also supports two general-purpose LEDs.

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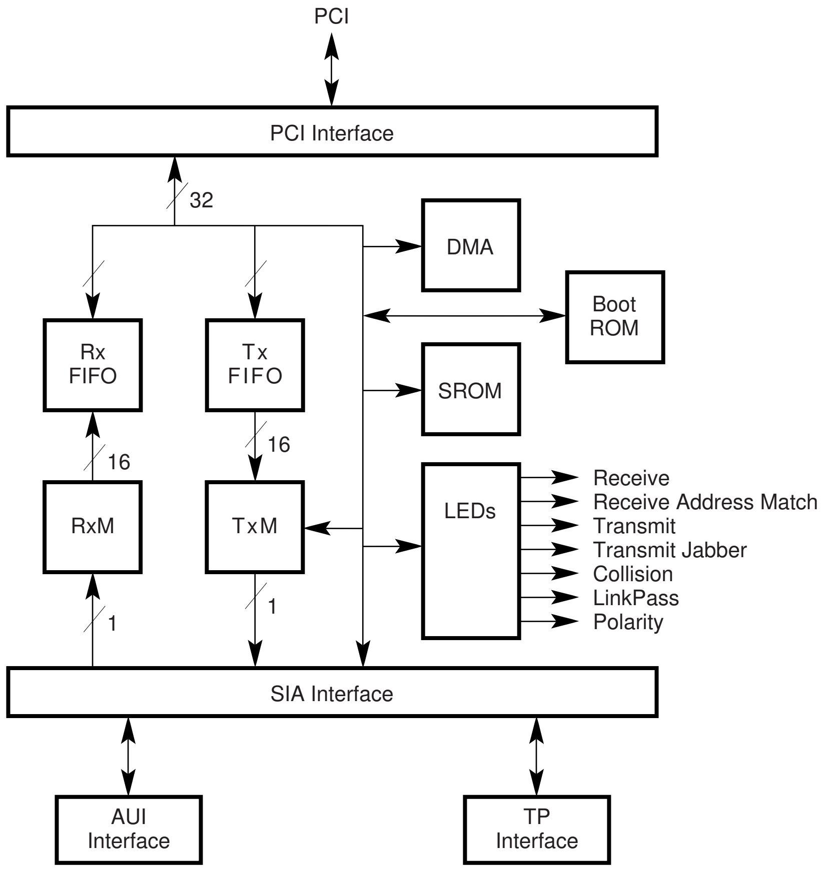
[1] Carrier-sense multiple access with collision detection
[2] Media access control

Figure 1 DECchip 21041 Microarchitecture



1.3 Features

The 21041 has the following features:

Note

Asterisks (*) indicate 21041 features that are not available on the 21040.

- Offers a single-chip Ethernet controller for PCI local bus
  - Provides a direct interface connection to PCI bus
  - Implements pinout order as recommended by the *PCI Local Bus Specification* to allow board layout within trace-length restriction*
  - Contains onchip integrated attachment unit interface (AUI) port and a 10BASE-T transceiver
- Implements the same architecture as DECchip 21040 to allow using unified drivers*
- Supports full-duplex operation and IEEE 802.3 autonegotiation algorithm of full-duplex and half-duplex environments*
- Provides upgradable boot ROM interface (FLASH or EEPROM) of 64K-, 128K-, or 256K-bytes*
- Contains serial ROM interface (suitable also for MicroWire EEPROM) for Ethernet ID address and optionally, other system parameters*
- Provides clock speed up to 33 megahertz, with no wait states on PCI master operation
- Enables powerful onchip DMA with programmable burst sizes of up to 32 longwords providing for low CPU utilization
- Implements unique, patent-pending intelligent arbitration between DMA channels preventing underflow or overflow and is optimized for full-duplex operation
- Incorporates a 16-bit, general-purpose timer*
- Contains two large (256-byte) independent receive and transmit FIFOs
- Supports either big or little endian byte ordering for buffers and descriptors
- Implements JTAG-compatible test access port with boundary-scan pins
- Provides full support of IEEE 802.3, ANSI 8802-3, and Ethernet standards

- Offers a unique, patented solution to Ethernet capture-effect problem
- Contains a variety of flexible address filtering modes
  - 16 perfect addresses
  - 512 hash-filtered, multicast addresses and one perfect address
  - 512 hash-filtered, physical addresses and multicast addresses
  - Inverse perfect filtering
- Supports seven LEDs: Receive, Receive Address Match, Transmit, Transmit Jabber, Collision, LinkPass, and Polarity.* It also supports two general-purpose LEDs.*
- Enables automatic detection and correction of 10BASE-T receive polarity
- Enables full autosensing between 10BASE-T, 10BASE2, and 10BASE5 ports*
- Provides external and internal loopback capability
- Provides a software-controllable, power-saving mode*
- Contains 3.3-volt complementary metal-oxide semiconductor (CMOS) device which interfaces to 5.0-volt or 3.3-volt logic
- Supports both PCI 5.0-volt and 3.3-volt signaling environments*

2 Pinout

The tables in this section provide a description of the pins and their respective signal definitions. Table 1 lists the tables in this section.

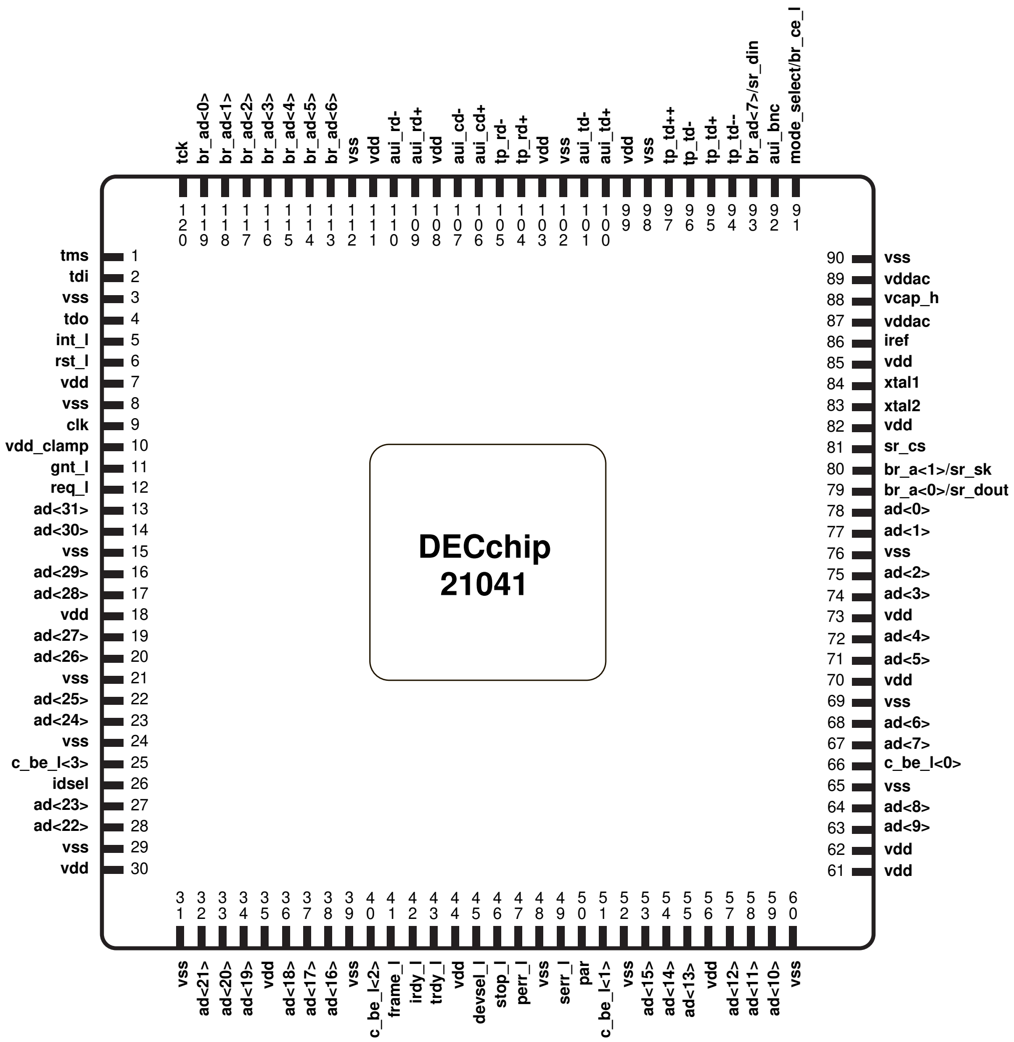
Table 1 Index to Pinout Tables

For this information . . .	Refer to . . .
Pin cross reference by logic signal	Table 2
Pin cross reference by power signal	Table 3
Quick pin reference	Table 4
Input pin reference	Table 5
Output pin reference	Table 6
Input/output pin reference	Table 7
Signal functions	Table 8

2.1 Pinout and Pin Descriptions

The 21041 is housed in the 120-pin plastic quad flat pack (PQFP). The 21041 uses all pins. Figure 2 shows the 21041 pinout.

Figure 2 DECchip 21041 Pinout Diagram (Top View)



2.2 Quick Pin Reference

Table 2 provides a pin cross reference listed by logic signal name. Table 3 provides a pin cross reference listed by power signal name. Table 4 is a quick pin reference that defines the logic signals.

Table 2 DECchip 21041 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
ad<0>	78	**ad<24>**	23
ad<1>	77	**ad<25>**	22
ad<2>	75	**ad<26>**	20
ad<3>	74	**ad<27>**	19
ad<4>	72	**ad<28>**	17
ad<5>	71	**ad<29>**	16
ad<6>	68	**ad<30>**	14
ad<7>	67	**ad<31>**	13
ad<8>	64	**aui_bnc**	92
ad<9>	63	**aui_cd–**	107
ad<10>	59	**aui_cd+**	106
ad<11>	58	**aui_rd–**	110
ad<12>	57	**aui_rd+**	109
ad<13>	55	**aui_td–**	101
ad<14>	54	**aui_td+**	100
ad<15>	53	**br_a<0>/sr_dout**	79
ad<16>	38	**br_a<1>/sr_sk**	80
ad<17>	37	**br_ad<0>**	119
ad<18>	36	**br_ad<1>**	118
ad<19>	34	**br_ad<2>**	117
ad<20>	33	**br_ad<3>**	116
ad<21>	32	**br_ad<4>**	115
ad<22>	28	**br_ad<5>**	114
ad<23>	27	**br_ad<6>**	113

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Table 2 (Cont.) DECchip 21041 Pin Cross Reference by Logic Signal

Signal	Location	Signal	Location
br_ad<7>/sr_din	93	**serr_l**	49
c_be_l<0>	66	**sr_cs**	81
c_be_l<1>	51	**stop_l**	46
c_be_l<2>	40	**tck**	120
c_be_l<3>	25	**tdi**	2
clk	9	**tdo**	4
devsel_l	45	**tms**	1
frame_l	41	**tp_rd–**	105
gnt_l	11	**tp_rd+**	104
idsel	26	**tp_td–**	96
int_l	5	**tp_td– –**	94
irdy_l	42	**tp_td+**	95
iref	86	**tp_td+ +**	97
mode_select /br_ce_l	91	**trdy_l**	43
par	50	**vcap_h**	88
perr_l	47	**xtal1**	84
req_l	12	**xtal2**	83
rst_l	6		

Table 3 DECchip 21041 Pin Cross Reference by Power Signal

Signal	Location	Signal	Location
vdd (3.3 V)	7, 18, 30, 35	**vss** (GND)	3, 8, 15, 21
	44, 56, 61, 62		24, 29, 31, 39
	70, 73, 82, 85		48, 52, 60, 65
	99, 103, 108, 111		69, 76, 90, 98
			102, 112
vdd_clamp	10		
vddac (3.3 V)	87, 89		

Table 4 lists a functional description of each of the 21041 signals. These signals are listed alphabetically. The functional grouping of each pin is listed in Section 2.4.

The following terms describe the 21041 pinout.

- **Address phase**

  The address and appropriate bus command are driven during this cycle.

- **Data phase**

  Data and the appropriate byte enable code are driven during this cycle.

- **_l**

  All pin names with the **_l** suffix are only asserted low.

Note

The following list describes the abbreviations used in the tables in this section.

I = Input
O = Output
I/O = Input/output
O/D = Open drain

Table 4 Quick Pin Reference

Signal	Type	Pin Number	Description
ad<31:00>	I/O	See Figure 2.	32-bit multiplexed PCI address and data lines. Address and data bits are multiplexed on the same pins. During the first clock cycle of a transaction, **ad<31:00>** contain a physical byte address (32 bits). During subsequent clock cycles, **ad<31:00>** contain data. A 21041 bus transaction consists of an address phase followed by one or more data phases. The 21041 supports both read and write bursts. Little and big endian byte ordering can be used.
aui_bnc	I/O	92	Attachment unit interface and BNC select line. When asserted high, the 10BASE5 (AUI) mode is selected. When asserted low, the 10BASE2 (BNC) mode is selected. This output pin is used mainly to enable the external BNC transceiver in 10BASE2 mode. This pin is an input pin in mode 0.
aui_cd–	I	107	Attachment unit interface receive collision differential negative data.
aui_cd+	I	106	Attachment unit interface receive collision differential positive data.
aui_rd–	I	110	Attachment unit interface receive differential negative data.
aui_rd+	I	109	Attachment unit interface receive differential positive data.
aui_td–	O	101	Attachment unit interface transmit differential negative data.
aui_td+	O	100	Attachment unit interface transmit differential positive data.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
br_a<0>/ sr_dout	I/O	79	Boot ROM address line bit 0. In a 256K-byte configuration, this pin also carries in two consecutive address cycles, boot ROM address bits 16 and 17. When the 21041 operates with the serial ROM, serial ROM data out (**sr_dout**) shifts the Ethernet identification address from the serial ROM device into the 21041. During operation with the external register, this pin is used for read and write control.
br_a<1>/ sr_sk	O	80	Boot ROM address line bit 1. This pin also latches the boot ROM address and control lines by the two external latches. When the 21041 operates with the serial ROM, **sr_sk** provides the serial ROM clock.
br_ad<6:0>	I/O	See Figure 2.	Boot ROM address and data multiplexed lines bits 6 through 0. In two consecutive address cycles, these lines contain the boot ROM address bits 6 through 2, **oe_l**, and **we_l** in the first cycle; and these lines contain boot ROM address bits 14 through 8 in the second cycle. During the data cycles, bits 6 through 0 contain data. The boot ROM address bits 6 through 0 can be connected directly to seven network event LEDs: Transmit, Collision, Receive Address Matching, Receive, TP Polarity, Transmit Jabber, and LinkPass respectively. During operation with the external register, these lines are used to carry data bits 6 through 0 to and from the external register.

(continued on next page)

Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
br_ad<7>/ sr_din	I/O	93	Boot ROM address and data multiplexed line bit 7. In two consecutive address cycles, this pin carries boot ROM address bits 7 and 15. During the data phase, it contains data. When the 21041 operates with the serial ROM, serial ROM data in (**sr_din**) serially shifts the Ethernet identification address from the 21041 into the serial ROM device. During operation with the external register, this pin is used to carry data bit 7 to and from the external register. When mode 0 (DECchip 21040) is selected, this pin must be tied to **vss**.
c_be_l<3:0>	I/O	See Figure 2.	Bits 0 through 3 of the bus command and byte enable lines. Bus command and byte enable are multiplexed on the same PCI pins. During the address phase of the transaction, **c_be_l<3:0>** provide the bus command. During the data phase, **c_be_l<3:0>** provide the byte enable. The byte enable determines which byte lines carry valid data. For example, **c_be_l<0>** applies to byte 0, and **c_be_l<3>** applies to byte 3. In all master and I/O operations, **c_be_l<3:0>** contain a value equal to a longword hexadecimal value of 0. In configuration operations, **c_be_l<3:0>** can contain any value; 21041 supports byte, word, and longword operations.
clk	I	9	The clock provides the timing for the 21041–related bus transactions. All the other bus signals are sampled on the rising edge of **clk**. The clock range is between 16 megahertz and 33 megahertz.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
devsel_l	I/O	45	The 21041 asserts device select when it is the target of the current bus access. When the 21041 is the initiator of the current bus access, it expects the target to assert **devsel_l** within 5 bus cycles, confirming the access. To accomplish this, the 21041 asserts this signal in a medium speed (within two bus cycles). If the target does not assert **devsel_l** within the required bus cycles, then the 21041 aborts the cycle.
frame_l	I/O	41	Frame is driven by the 21041 (bus initiator) to indicate the beginning and duration of an access. When **frame_l** asserts, it indicates the beginning of a bus transaction. While **frame_l** is asserted, data transfers continue. When **frame_l** is deasserted, it indicates that the next data phase is the final data phase transaction.
gnt_l	I	11	Bus grant asserts to indicate to the 21041 that access to the bus is granted.
idsel	I	26	Initialization device select asserts to act as a chip select during configuration read or write transactions.
int_l	O/D	5	Interrupt request asserts when one of the appropriate bits of CSR5 sets and causes an interrupt, provided that the corresponding mask bit in CSR7 is not asserted. **int_l** deasserts by writing a 1 into the appropriate CSR5 bit. If more than one interrupt bit is asserted in CSR5, then the host clears only the interrupt bit that was acknowledged, **int_l** deasserts for one cycle and then asserts again. This process continues until all interrupts are acknowledged. When deasserted, this pin should be pulled up by an external resistor.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
irdy_l	I/O	42	Initiator ready indicates the bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **irdy_l** and target ready (**trdy_l**) are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21041 is the bus initiator, **irdy_l** is asserted during write operations to indicate that valid data is present on **ad<31:00>**. During read operations, the 21041 asserts **irdy_l** to indicate that it is ready to accept data.
iref	I	86	Current reference input for the analog phase-locked loop (PLL) logic.
mode_select/ br_ce_l	I/O	91	Selects either mode 0 (DECchip 21040) or mode 1 (DECchip 21041) operation. When this pin is tied to VSS, mode 0 operation is selected. When this pin is not connected (internally pulled up), mode 1 operation is selected. When a hardware or software reset is detected, the 21041 senses this input and sets the mode of operation accordingly. When mode 1 operation is selected, this pin changes its functionality, and it is actually the boot ROM or the external register chip enable (**br_ce_l**) output pin.
par	I/O	50	Parity is calculated by the 21041 as an even parity bit for the **ad<31:00>** and **c_be_l<3:0>** lines. During address and data phases, **par** is calculated on all the **ad** and **c_be_l** lines whether or not any of these lines carry meaningful information.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
perr_l	I/O	47	Parity error asserts when a data parity error is detected. When the 21041 is the bus initiator and a parity error is detected, the 21041 asserts both CSR5 bit 13 (system error) and CFCS bit 9 (**serr_l** enable) and completes the current data burst transaction, then stops its operation. After the host clears the system error, the 21041 continues its operation. When the 21041 is the bus target and a parity error is detected, the 21041 asserts **perr_l**.
req_l	O	12	Bus request is asserted by the 21041 to indicate to the bus arbiter that it wants to use the bus.
rst_l	I	6	Resets the 21041 to its initial state. This signal must be asserted for at least 10 active PCI clock cycles. When in the reset state, all PCI port output pins are put into tristate and all open drain (O/D) signals are floated.
serr_l	O/D	49	If an address parity error is detected and CFCS bit 31 (detected parity error) is enabled, then 21041 asserts both **serr_l** (system error) and CFCS bit 30 (signal system error). When an address parity error is detected, system error asserts two clocks after the failing address. When deasserted, this pin should be pulled up by an external resistor.
sr_cs	O	81	Serial ROM chip select asserts when the 21041 accesses the serial ROM.
stop_l	I/O	46	Stop indicator indicates that the current target is requesting the bus initiator to stop the current transaction. The 21041 responds to the assertion of **stop_l** when it is the bus initiator, either to disconnect, retry, or abort.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
tck	I	120	JTAG clock shifts state information and test data into and out of the 21041 during JTAG test operations.
tdi	I	2	JTAG data in is used to serially shift test data and instructions into the 21041 during JTAG test operations.
tdo	O	4	JTAG data out pin is used to serially shift test data and instructions out of the 21041 during JTAG test operations.
tms	I	1	JTAG test mode select controls the state operation of JTAG testing in the 21041.
tp_rd–	I	105	Twisted-pair negative differential receive data.
tp_rd+	I	104	Twisted-pair positive differential receive data.
tp_td– **tp_td– –**	O	See Figure 2.	Twisted-pair negative differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21041 with equalization to compensate for intersymbol interference on the twisted-pair medium.
tp_td+ **tp_td+ +**	O	See Figure 2.	Twisted-pair positive differential transmit data. The positive and negative differential transmit data outputs are resistively combined outside the 21041 with equalization to compensate for intersymbol interference on the twisted-pair medium.

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Table 4 (Cont.) Quick Pin Reference

Signal	Type	Pin Number	Description
trdy_l	I/O	43	Target ready indicates the target agent's ability to complete the current data phase of the transaction. A data phase is completed on any clock when both **trdy_l** and initiator ready (**irdy_l**) are asserted. Wait cycles are inserted until both **irdy_l** and **trdy_l** are asserted together. When the 21041 is the bus initiator, **trdy_l** is asserted by the bus target on the read operation indicating that valid data is present on **ad<31:00>**. During a write cycle, it indicates that the target is prepared to accept data.
vcap_h	I	88	Capacitor input for analog PLL logic.
vdd	I	See Figure 2.	3.3-volt supply input voltage.
vddac	I	See Figure 2.	3.3-volt supply input for analog PLL logic.
vdd_clamp	I	10	Supplies +5 volts or +3.3 volts reference for the clamp logic.
vss	–	See Figure 2.	Ground pin.
xtal1	I	84	Crystal oscillator input.
xtal2	O	83	Crystal feedback output pin used for crystal connections only. If this pin is unused, then do not connect it.

2.3 Pin Reference Tables

There are three pin reference tables:

- Table 5 lists the input pins.
- Table 6 lists the output pins.
- Table 7 lists the input/output pins.

Table 5 Input Pin Reference

Signal	Signal
aui_cd–	**tck**
aui_cd+	**tdi**
aui_rd–	**tms**
aui_rd+	**tp_rd–**
clk	**tp_rd+**
gnt_l	**vcap_h**
idsel	**vdd**
iref	**vddac**
rst_l	**vdd_clamp**
	xtal1

Table 6 Output Pin Reference

Signal	Signal
aui_td–	**tdo**
aui_td+	**tp_td–**
br_a<1>/sr_sk	**tp_td– –**
int_l	**tp_td+**
req_l	**tp_td+ +**
sr_cs	**xtal2**

Table 7 Input/Output Pin Reference

Signal	Signal
ad<31:00>	**irdy_l**
aui_bnc	**mode_select/br_ce_l**
br_a<0>/sr_dout	**par**
br_ad<6:0>	**perr_l**
br_ad<7>/sr_din	**serr_l**
c_be_l<3:0>	**stop_l**
devsel_l	**trdy_l**
frame_l	

2.4 Signal Grouping by Function

Table 8 lists the signals according to their interface function.

Table 8 Signal Functions

Interface	Function	Signal
PCI	Address and data	**ad<31:00>**
	Arbitration	**gnt_l**, **req_l**
	Bus command and byte enable	**c_be_l<3:0>**
	Control	**frame_l, irdy_l, stop_l, trdy_l**
	Device select	**devsel_l, idsel**
	Error reporting	**perr_l, serr_l**
	Interrupt	**int_l**
	Parity	**par**
	System	**clk, rst_l**
Network connection	Analog PLL logic	**iref, vcap_h**
	AUI collision data	**aui_cd–, aui_cd+**
	AUI transmit and receive data	**aui_rd–, aui_rd+, aui_td–, aui_td+**
	10BASE5/10BASE2 select	**aui_bnc**
	Crystal oscillator	**xtal1, xtal2**
	Twisted-pair transmit and receive data	**tp_rd–, tp_rd+, tp_td–, tp_td– –, tp_td+, tp_td+ +**
Power and diagnostic	3.3-volt and 5-volt supply input	**vdd, vddac, vdd_clamp**
	Ground	**vss**
Test access port	JTAG test operations	**tck, tdi, tdo, tms**
Ethernet ID ROM and boot ROM	Address serial ROM and boot ROM interface	**br_ad<7>/sr_din**, **br_ad<6:0>**, **sr_cs**, **br_a<1>/sr_sk**, **br_a<0>/sr_dout**
Chip mode	Select mode 1, 0	**mode_select/br_ce_l**

3 Electrical and Environmental Specifications

This section contains the electrical and environmental specifications of the 21041. The test conditions for the specified values are as follows unless otherwise indicated:

- Temperature (Ta): 70°C
- Power supply voltage (**vdd**): 3.3 V
- Power supply voltage (**vddac**): 3.3 V
- Reference voltage (**vdd_clamp**): 3.3 V or 5.0 V
- Ground (**vss**): 0 V

3.1 Voltage Limit Ratings

Table 9 lists the voltage limit ratings.

Table 9 Voltage Limit Ratings

Parameter	Minimum	Maximum
Power supply voltage	+3.0 V	+3.6 V
vdd_clamp (5.0 V)	+4.75 V	+5.25 V
vdd_clamp (3.3 V)	+3.0 V	+3.6 V
ESD protection voltage	–	2000 V

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21041. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21041.

3.2 Temperature Limit Ratings

Table 10 lists the temperature limit ratings.

Table 10 Temperature Limit Ratings

Parameter	Minimum	Maximum
Storage temperature	–55°C	+125°C
Operating temperature	0°C	70°C

Caution

Stresses greater than the maximum or less than the minimum ratings can cause permanent damage to the 21041. Exposure to the maximum or minimum ratings for extended periods of time lessen the reliability of the 21041.

3.3 Supply Current and Power Dissipation

The values in Table 11 are estimates based on a PCI clock frequency of 33 megahertz and a network clock frequency of 10 megahertz.

Table 11 Supply Current and Power Dissipation

Symbol	Conditions	Typical	Maximum	Units
IDD	VDD=3.6 V, Ta=70°C	150	190	mA
Normal power mode	VDD=3.6 V, Ta=70°C	0.54	0.68	W
Snooze power mode[1]	VDD=3.6 V, Ta=70°C	0.33	0.41	W
Sleep power mode[1]	VDD=3.6 V, Ta=70°C	0.25	0.32	W

[1]Refer to the *DECchip 21041 Ethernet LAN Controller for PCI Hardware Reference Manual* for a description of sleep mode and snooze mode.

3.4 PCI Bus Electrical Specifications

This section contains information about electrical characteristics for the 21041 input and output pins of the PCI.

3.4.1 PCI I/O Voltage Specifications

The 21041 meets the I/O voltage specifications listed in Table 12 and Table 13.

Table 12 I/O Voltage Specifications for 5.0-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	–	2.0 V	**vdd_clamp** + 0.5 V
Vil	Input low voltage	–	–0.5 V	0.8 V
Ii[1]	Input leakage current	0.5 V <Vin<2.7 V	–	±20 μA
Voh	Output high voltage	Iout=–2mA	2.4 V	–
Vol[2]	Output low voltage	Iout=3mA, 6mA	–	0.55 V
Cap[3]	Pin capacitance	–	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Signals without pullup resistors must have 3 milliamps low output current. Signals requiring pullup resistors (including **frame_l, trdy_l, irdy_l, devsel_l, stop_l, serr_l, and perr_l**) must have 6 milliamps.

[3]Parameter design guarantee.

Table 13 I/O Voltage Specifications for 3.3-Volt Levels

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input high voltage	–	0.475***vdd_clamp**	**vdd_clamp** + 0.5 V
Vil	Input low voltage	–	–0.5 V	0.325***vdd_clamp**
Ii[1]	Input leakage current	0.0 V <Vin<**vdd_clamp**	–	±10 µA
Voh	Output high voltage	Iout=–500 µA	0.9***vdd_clamp**	–
Vol	Output low voltage	Iout=1500 µA	–	0.1***vdd_clamp**
Cap[2]	Pin capacitance	–	5 pF	8 pF

[1]Input leakage currents include high-impedance output leakage for all bidirectional buffers with tristate outputs.

[2]Parameter design guarantee.

3.4.2 PCI Reset

PCI reset (**pci_rst**) is an asynchronous signal that must be active for at least 10 PCI clock (**pci_clk**) cycles. Figure 3 shows the PCI reset timing characteristics, and Table 14 lists the PCI reset signal limits.

Figure 3 PCI Reset Timing Diagram

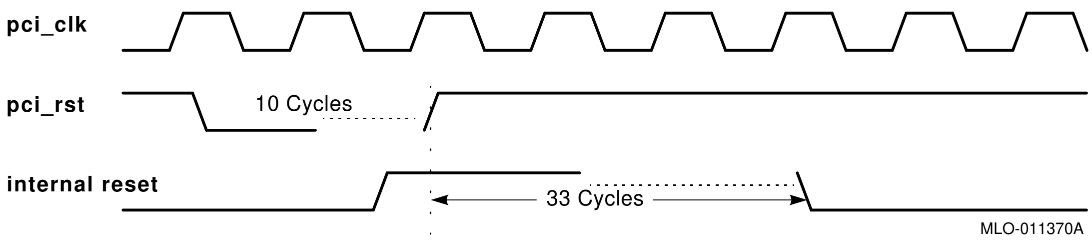


Table 14 PCI Reset Timing Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Trst	**pci_rst** pulse width	10*Tcycle	–	**pci_clk** active

3.4.3 PCI Clock Specifications

The standard clock frequency range for the PCI is between 16 megahertz and 33 megahertz. Figure 4 shows the PCI clock timing characteristics, and Table 15 lists the frequency-derived clock specifications.

Figure 4 PCI Clock Timing Diagram

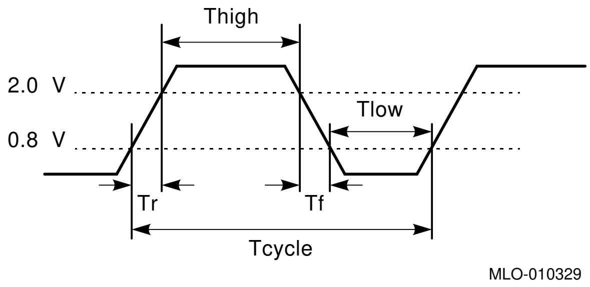


Table 15 PCI Clock Timing Specifications

Symbol	Parameter	Minimum	Maximum	Notes
Tcycle	Cycle time	30 ns	62.5 ns	–
Thigh	**pci_clk** high time	0.4*Tcycle	0.6*Tcycle	At 2 V
Tlow	**pci_clk** low time	0.4*Tcycle	0.6*Tcycle	At 0.8 V
Tr/Tf	**pci_clk** slew rate[1]	1 V/ns	4 V/ns	–

[1]Rise and fall times are specified in terms of the edge rate measured in V/ns. Parameter design guarantee.

3.4.4 Other PCI Signals

Figure 5 shows the timing diagram characteristics, and Table 16 lists the other PCI signal specifications.

Figure 5 Timing Diagram for Other PCI Signals

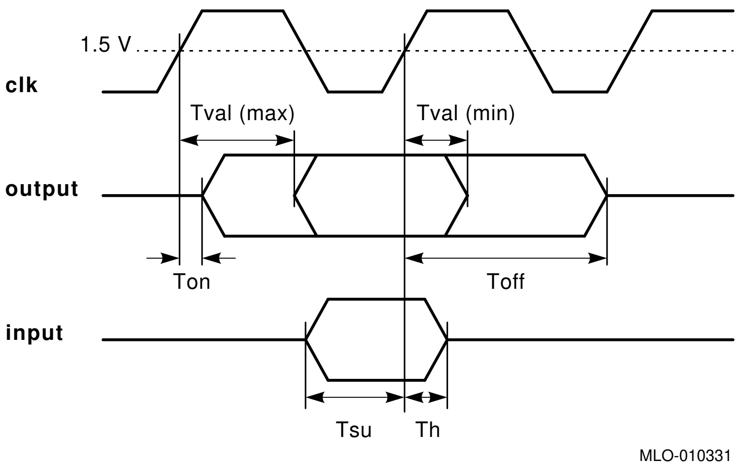


Table 16 Other PCI Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Conditions
Tval	**clk**-to-signal valid delay	2 ns	11 ns	Cload = 50 pF
Ton[1]	Float-to-active delay from **clk**	2 ns	–	–
Toff[1]	Active-to-float delay from **clk**	–	28 ns	–
Tsu	Input signal valid setup time before **clk**	7 ns	–	–
Th	Input signal hold time from **clk**	0 ns	–	–
Tr[1]	Unloaded output rise time	1.0 V/ns	4.0 V/ns	0.4 V to 2.4 V (5.0-V levels), 0.2***vdd_clamp** to 0.6***vdd_clamp** (3.3-V levels)
Tf[1]	Unloaded output fall time	1.0 V/ns	4.0 V/ns	2.4 V to 0.4 V (5.0-V levels), 0.6***vdd_clamp** to 0.2***vdd_clamp** (3.3-V levels)

[1]Parameter design guarantee.

3.5 AUI and Twisted-Pair dc Specifications

Table 17 lists the dc specifications for the AUI and twisted-pair parts of the SIA.

Table 17 AUI and Twisted-Pair dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
AUI Pins					
V_{od}	Transmit differential output voltage (**aui_td±**)	78 Ω termination	±550	±1200	mV
V_{odi}[1]	Transmit differential output idle voltage (**aui_td±**)	78Ω termination	–40	+40	mV
I_{odi}[1]	Transmit differential output idle current (**aui_td±**)	78Ω termination	–1	+1	mA
V_{asq+}[1]	Differential positive squelch threshold (**aui_rd±**)	–	175	275	mV
V_{asq-}[1]	Differential negative squelch threshold (**aui_rd±** and **aui_cd±**)	–	–275	–175	mV
V_{odu}[1]	Transmit differential output undershoot voltage on return to zero (**aui_td±**)	78Ω termination	–	–100	mV
Twisted-Pair Interface Pins					
V_{toh}	Output high voltage (**tp_td±** and **tp_td±±**)	I_{oh} = –25 mA	+ 2.5	V_{dd}	V
V_{tol}	Output low voltage (**tp_td±** and **tp_td±±**)	I_{ol} = 25 mA	V_{ss}	+ 0.5	V
V_{tsq+}[1]	Differential positive squelch threshold (**tp_rd±**)	–	300	520	mV
V_{tsq-}[1]	Differential negative squelch threshold (**tp_rd±**)	–	–520	–300	mV
V_{tdif}[1]	Differential input voltage range (**tp_rd±**)	–	–3.1	3.1	V

[1]Parameter design guarantee.

3.6 Serial Interface Attachment Specifications

This section describes the dc specifications and timing limits of the SIA unit.

3.6.1 Serial Clock dc Specifications

Table 18 lists the dc specifications for the two serial clock pins: **xtal1 and xtal2**.

Table 18 Serial Clock (XTAL) dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_i	Input leakage current	0.0 <Vin<**vdd**	–	±10	µA

3.6.2 Serial Clock Timing

Figure 6 shows the serial clock (TTL or CMOS) timing characteristics, and Table 19 lists the serial clock timing specifications.

Figure 6 Serial Clock (XTAL) Timing Diagram

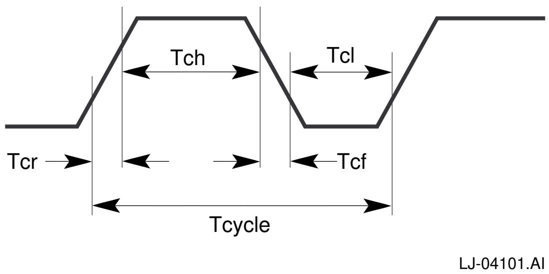


Table 19 Serial Clock (XTAL) Timing Specifications

Symbol	Parameter	Minimum	Maximum
Tcr[1]	Rise time	–	4 ns
Tcf[1]	Fall time	–	4 ns
Tcycle	Cycle time	49.995 ns	50.005 ns
Tch	Clock high time	0.4*Tcycle	0.6*Tcycle
Tcl	Clock low time	0.4*Tcycle	0.6*Tcycle

[1]Parameter design guarantee.

3.6.3 Internal SIA Mode AUI Timing—Transmit

Figure 7 shows the internal SIA transmit timing characteristics for the AUI, and Table 20 lists the internal SIA transmit timing limits for the AUI.

Figure 7 Internal SIA Mode AUI Timing Diagram—Transmit

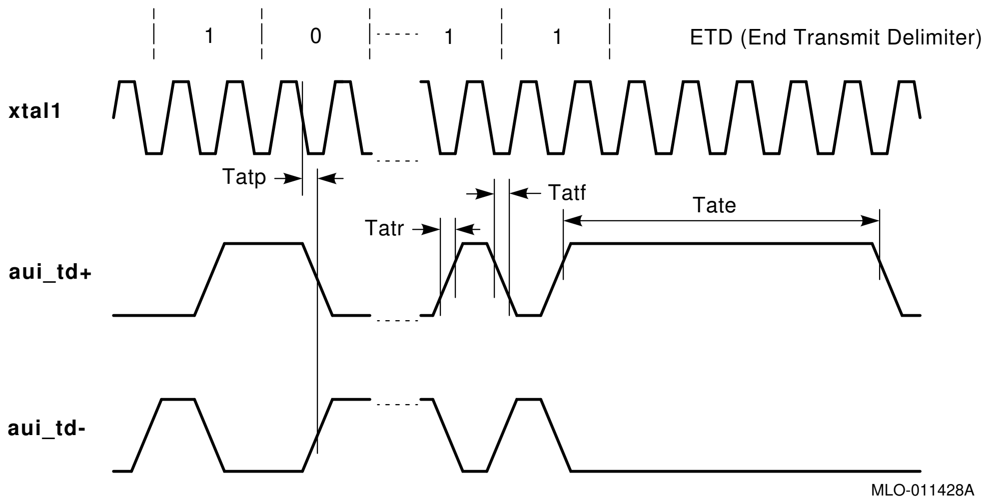


Table 20 Internal SIA Mode AUI Timing Specifications—Transmit

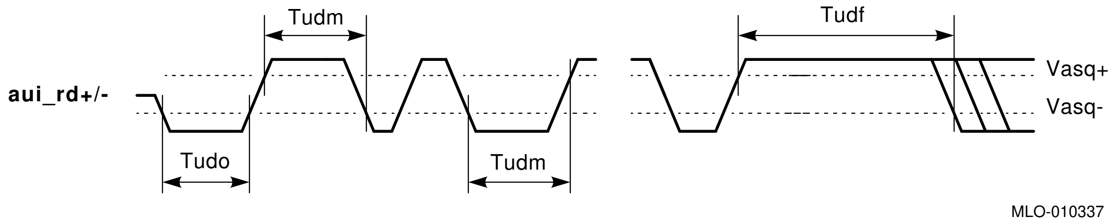
Symbol	Definition	Minimum	Maximum	Units
Tatp	**aui_td+, aui_td–** propagation delay from **xtal1** fall	–	30	ns
Tatr[1]	**aui_td+, aui_td–** rise time	2	8	ns
Tatf[1]	**aui_td+, aui_td–** fall time	2	8	ns
Tatm[1]	**aui_td+, aui_td–** rise and fall time mismatch (not shown)	–	1	ns
Tate	**aui_td±** end transmit delimiter length	345	405	ns

[1]Parameter design guarantee.

3.6.4 Internal SIA Mode AUI Timing—Receive

Figure 8 shows the internal SIA receive timing characteristics for the AUI, and Table 21 lists the internal SIA receive timing limits for the AUI.

Figure 8 Internal SIA Mode AUI Timing Diagram—Receive



3.6.5 Internal SIA Mode AUI Timing—Collision

Figure 9 shows the internal SIA collision timing characteristics for the AUI, and Table 21 lists the internal SIA collision timing limits for the AUI.

Figure 9 Internal SIA Mode AUI Timing Diagram—Collision

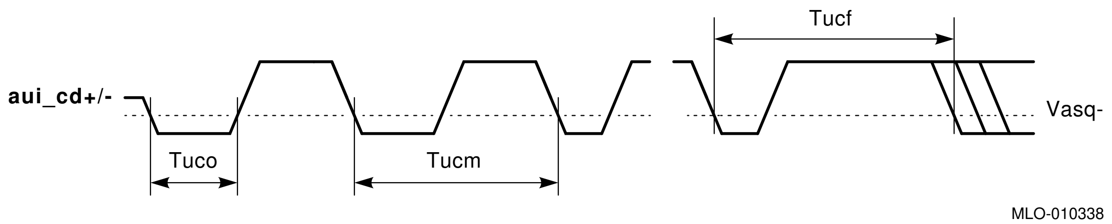


Table 21 Internal SIA Mode AUI Timing Specifications—Receive and Collision

Symbol	Definition	Minimum	Maximum	Units
Tudo	**aui_rd±** start of frame pulse width	15	20	ns
Tudm	**aui_rd±** delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tudf	**aui_rd±** delay from last squelch crossing recognized as end of packet	150	–	ns
Tuco	**aui_cd±** start of collision pulse width	20	25	ns
Tucm	**aui_cd±** delay between squelch crossings not recognized as end of collision	–	140	ns
Tucf	**aui_cd±** delay from last squelch crossing recognized as end of collision	150	–	ns

3.6.6 Internal SIA Mode 10BASE-T Interface Timing—Transmit

Figure 10 shows the internal SIA transmit timing characteristics for the 10BASE-T interface, and Table 22 lists the internal SIA transmit limits.

Figure 10 Internal SIA Mode 10BASE-T Interface Timing Diagram—Transmit

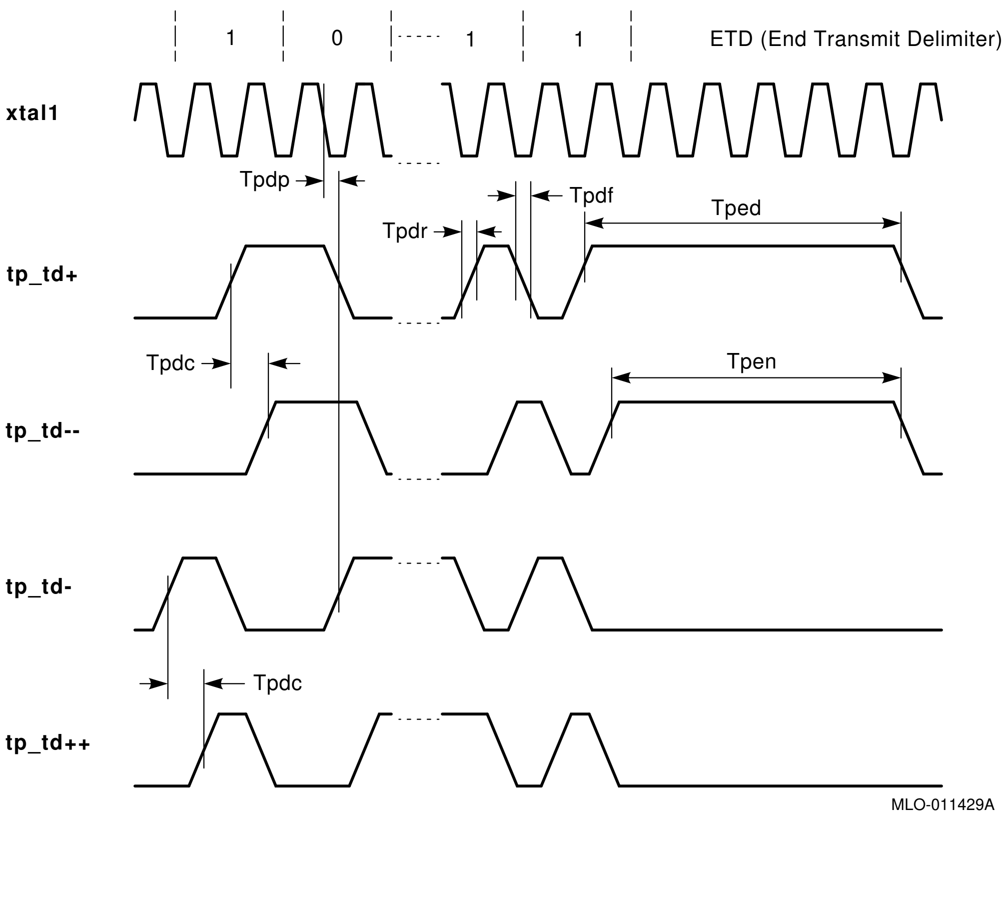


Table 22 Internal SIA Mode 10BASE-T Interface Timing Specifications—Transmit

Symbol	Definition	Minimum	Maximum	Units
Tpdp	**tp_td+, tp_td–** propagation delay from **xtal1** fall	–	30	ns
Tpdr[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** rise time	2	8	ns
Tpdf[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** fall time	2	8	ns
Tpdm[1]	**tp_td+, tp_td++, tp_td–, tp_td– –** rise and fall time mismatch (not shown)	–	1	ns
Tpdc	**tp_td+** to **tp_td– –** and **tp_td–** to **tp_td++** delay	46	54	ns
Tped	**tp_td±** end transmit delimiter length	295	355	ns
Tpen	**tp_td++/– –** end transmit delimiter length	245	305	ns

[1]Parameter design guarantee.

3.6.7 Internal SIA Mode 10BASE-T Interface Timing—Receive

Figure 11 shows the internal SIA receive timing characteristics for the 10BASE-T interface, and Table 23 lists the internal SIA receive limits for the 10BASE-T interface.

Figure 11 Internal SIA Mode 10BASE-T Interface Timing Diagram—Receive

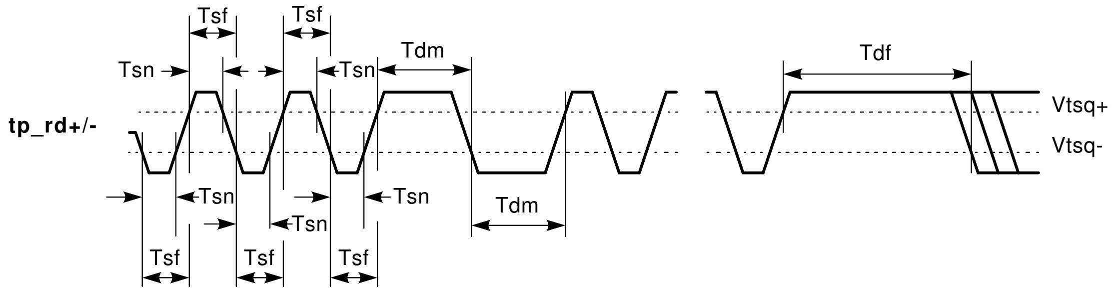


Table 23 Internal SIA Mode 10BASE-T Interface Timing Specifications—Receive

Symbol	Definition	Minimum	Maximum	Units
Tsn	**tp_rd±** start of frame pulse width during smart squelch operation	15	20	ns
Tsf	**tp_rd±** maximum delay between opposite squelch crossings to not turn smart squelch off	140	150	ns
Tdm	**tp_rd±** delay between opposite squelch crossings not recognized as end of packet	–	140	ns
Tdf	**tp_rd±** delay from last squelch crossing recognized as end of packet	150	–	ns

3.6.8 Internal SIA Mode 10BASE-T Interface Timing—Idle Link Pulse

Figure 12 shows the internal SIA idle link pulse timing characteristics for the 10BASE-T interface, and Table 24 lists the internal SIA idle link pulse limits for the 10BASE-T interface.

Figure 12 Internal SIA Mode 10BASE-T Interface Timing Diagram—Idle Link Pulse

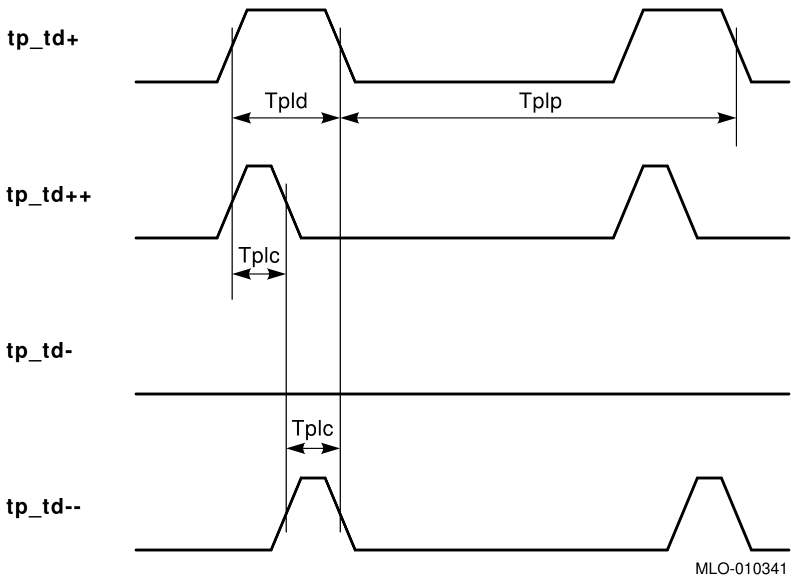


Table 24 Internal SIA Mode 10BASE-T Interface Timing Specifications—Idle Link Pulse

Symbol	Definition	Minimum	Maximum	Units
Tpld	**tp_td+** idle link pulse width	80	120	ns
Tplc	**tp_td++** and **tp_td– –** idle link pulse width	40	60	ns
Tplp	Idle link pulse period	8	24	ms

3.7 Joint Test Action Group — Test Access Port

This section provides the joint test action group (JTAG) test access port specifications.

3.7.1 JTAG dc Specifications

Table 25 lists the dc specifications for the JTAG pins.

Table 25 JTAG dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_i	Input leakage current (**tck**)	0.0 <Vin<**vdd**	–	±20	μA
I_{ip}	Input leakage current on pins with internal pullups (**tdi** and **tms**)	0.0 <Vin<**vdd**	–	+20/–1500[1]	μA
I_{oz}	Tristate output leakage current (**tdo**)	0.0 <Vout<**vdd**	–	±20	μA

[1]For **tdi** and **tms** pins that have internal pullups, the leakage current can get to 1.5 mA when Vin = 0 V.

3.7.2 JTAG Boundary-Scan Timing

Figure 13 shows the JTAG boundary-scan timing, and Table 26 lists the interface signal timing relationships.

Figure 13 JTAG Boundary-Scan Timing Diagram

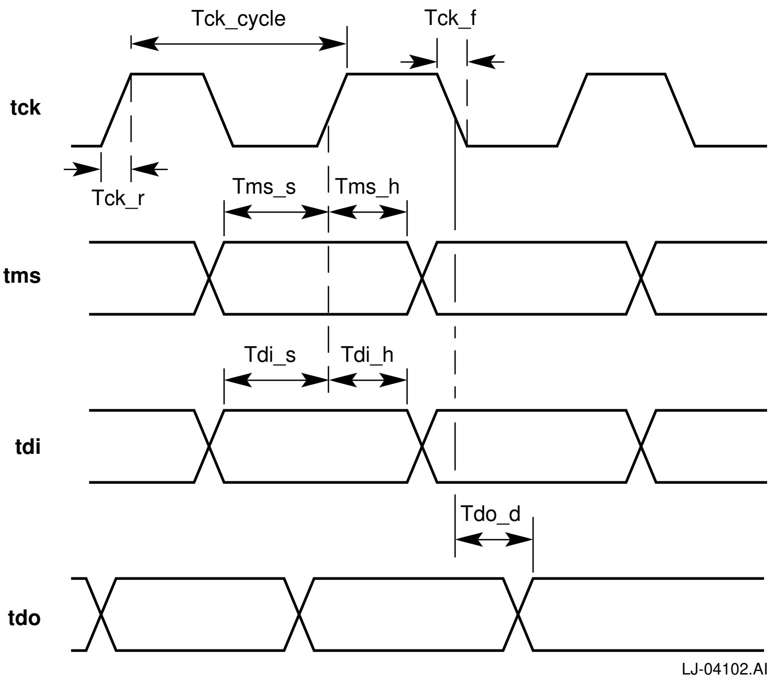


Table 26 JTAG Interface Signal Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tms_s	**tms** setup time	20	–	ns
Tms_h	**tms** hold time	5	–	ns
Tdi_s	**tdi** setup time	20	–	ns
Tdi_h	**tdi** hold time	5	–	ns
Tdo_d	**tdo** delay time	–	20	ns
Tck_r[1]	**tck** rise time	–	3	ns
Tck_f[1]	**tck** fall time	–	3	ns
Tck_cycle	**tck** cycle time	90	–	ns

[1]Parameter design guarantee.

3.8 Boot ROM, Serial Rom, and LED Port Specification

Table 27 lists the dc specifications for the boot ROM, serial ROM, and the LED multiplexed port. These specifications apply in any mode in which the port is used.

Table 27 Boot ROM, Serial ROM, and LED Port dc Specifications

Symbol	Definition	Conditions	Minimum	Maximum	Units
V_{oh}	Output high voltage	I_{oh} = –4 mA	2.4	–	V
V_{ol}	Output low voltage	I_{ol} = 4 mA	–	0.4	V
V_{ih}	Input high voltage	–	2.0	–	V
V_{il}	Input low voltage	–	–	0.8	V
I_{oz}	Maximum tristate output leakage current	$V_{out} = V_{dd}$ or V_{ss}	–10	10	μA

3.9 LED Timing

Figure 14 shows the stretching function for a sample internal signal that is reflected by an LED. It also shows how this function affects the time that the LED is on. Table 28 lists the stretching function timing specification.

Figure 14 LED Signal Stretching Function Timing Diagram

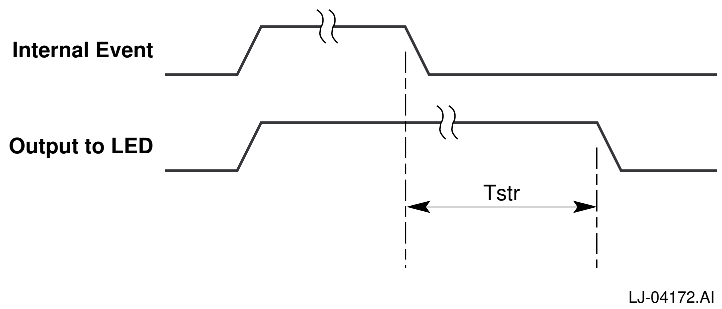


Table 28 LED Signal Stretching Function Timing Specifications

Symbol	Definition	Minimum	Maximum	Units
Tstr[1]	Stretch time from internal event fall time	52	78	ms

[1]Parameter design guarantee.

3.10 Boot ROM Port Timing

This section describes the boot ROM port timing.

3.10.1 Boot ROM Read Timing

Figure 15 shows the boot ROM read timing characteristics, and Table 29 lists the boot ROM read timing limits.

Figure 15 Boot ROM Read Timing Diagram

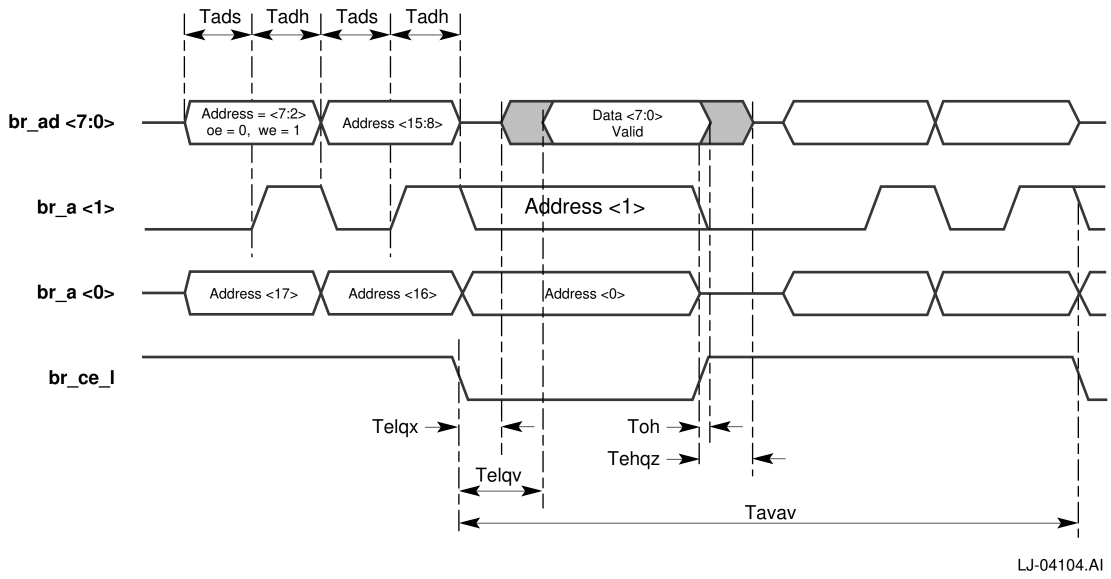


Table 29 Boot ROM Read Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Read cycle time	120	–	ns
Tavqv	Address to output delay	–	120	ns
Telqv	**br_ce_l** to output delay	–	120	ns
Telqx[1]	**br_ce_l** to output low impedance	0	–	ns
Tehqz[1]	**br_ce_l** going high to output high impedance	–	55	ns
Toh	Output hold from **br_ce_l** change	0	–	ns
Tads	Address setup to latch enable high	30	–	ns
Tadh	Address hold from latch enable high	30	–	ns

[1]Parameter design guarantee.

3.10.2 Boot ROM Write Timing

Figure 16 shows the boot ROM write timing characteristics, and Table 30 lists the boot ROM write timing limits.

Figure 16 Boot ROM Write Timing Diagram

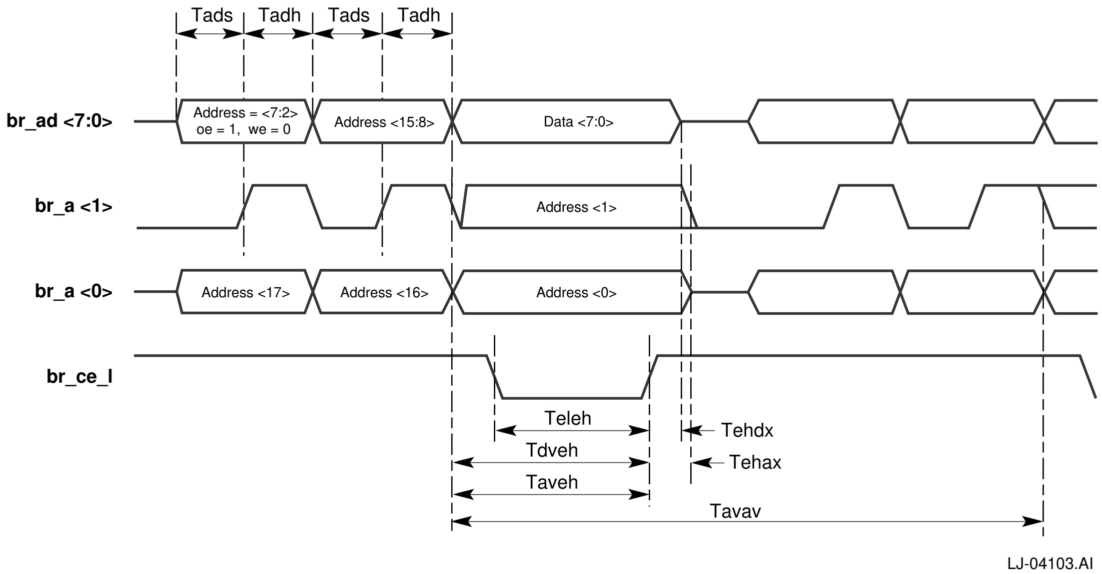


Table 30 Boot ROM Write Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Tavav	Write cycle time	120	–	ns
Teleh	**br_ce_l** pulse width	70	–	ns
Taveh	Address setup to **br_ce_l** going high	50	–	ns
Tdveh	Data setup to **br_ce_l** going high	50	–	ns
Tehdx	Data hold from **br_ce_l** going high	10	–	ns
Tehax	Address hold from **br_ce_l** high	15	–	ns
Tads	Address setup to latch enable high	30	–	ns
Tadh	Address hold from latch enable high	30	–	ns

3.11 Ethernet ID Port Serial ROM Timing

Figure 17 shows the Ethernet ID port serial ROM timing characteristics, and Table 31 lists the Ethernet ID port serial ROM timing limits.

Figure 17 Ethernet ID Port Timing Diagram

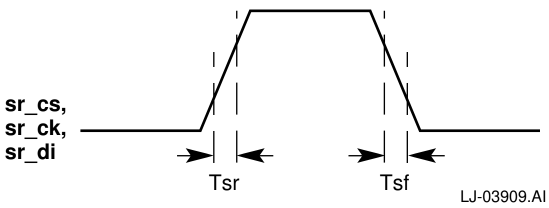


Table 31 Ethernet ID Port Timing Specifications

Symbol	Definition	Minimum	Maximum	Units
Tsr[1]	Rise time	–	10	ns
Tsf[1]	Fall time	–	10	ns

[1]Parameter design guarantee.

3.12 External Register Timing

Figure 18 shows the external register read timing characteristics, and Figure 19 shows its write timing characteristics. Table 32 lists the external register timing specifications for both read and write operations.

Figure 18 External Register Read Timing Diagram

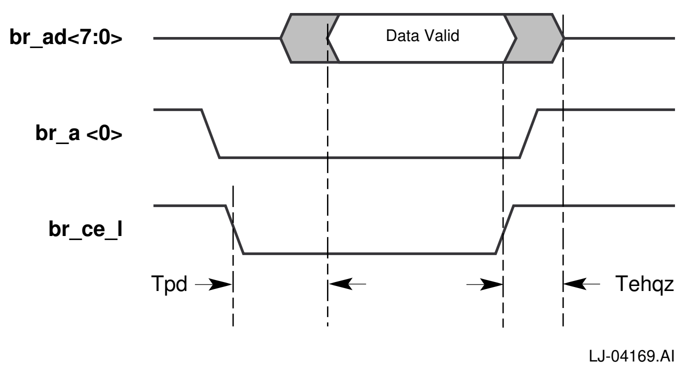


Figure 19 External Register Write Timing Diagram

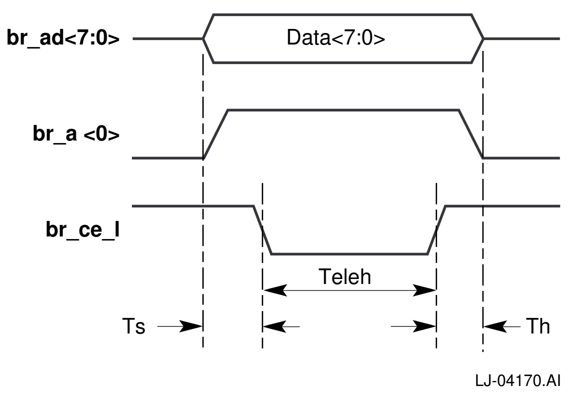


Table 32 External Register Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units
Teleh	**br_ce_l** pulse width	120	–	ns
Read Timing				
Tpd	**br_ce_l** low to **br_ad<7:0>** valid high	–	20	ns
Tehqz[1]	**br_ce_l** high to **br_ad<7:0>** high impedance	–	20	ns
Write Timing				
Ts	Data setup time prior to **br_ce_l**	30	–	ns
Th	Data hold after **br_ce_l** high	30	–	ns

[1]Parameter design guarantee.

4 Mechanical Specifications

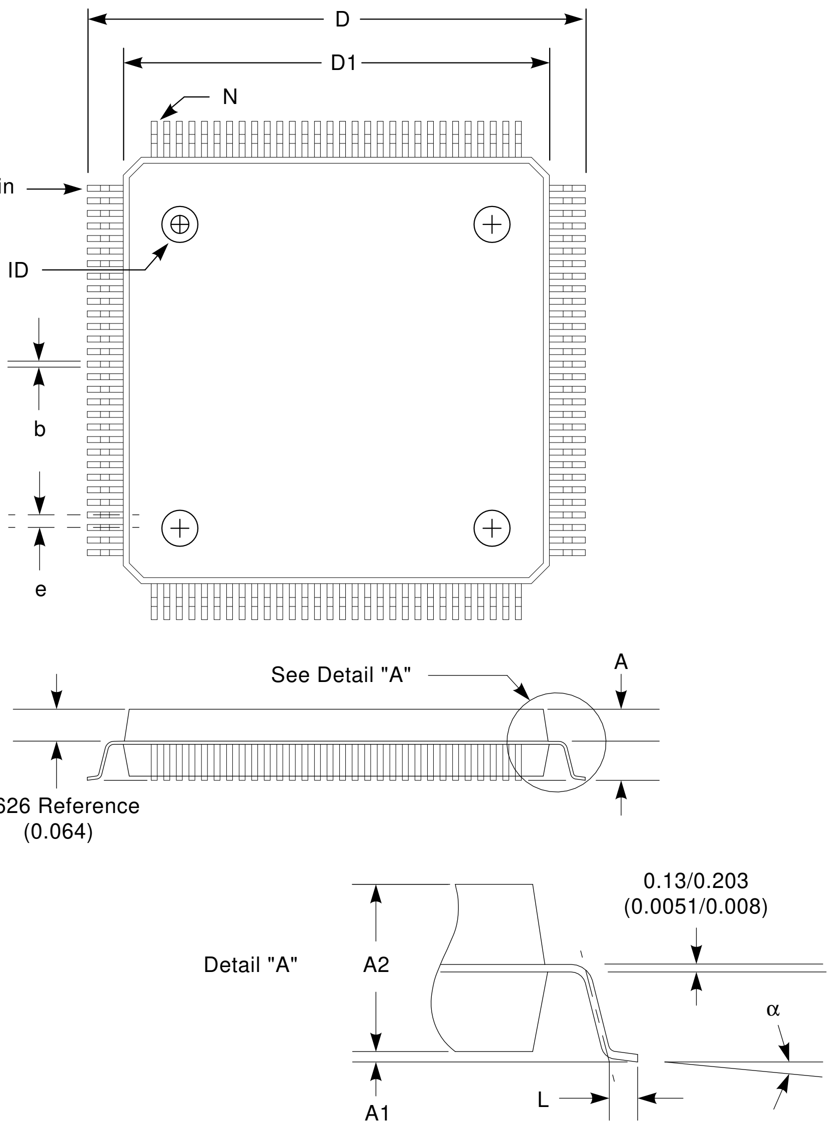
The 21041 is contained in a 120-pin plastic quad flat pack (PQFP). Table 33 lists the mechanical specifications, and Figure 20 shows the mechanical layout of the 21041.

Table 33 Mechanical Features

Item	Minimum[1]	Nominal[1]	Maximum[1]
A	–	–	4.07
A1	0.25	–	–
A2	3.17	3.37	3.67
D	–	31.20	–
D1	–	28.00 BSC	–
L	0.65	0.80	1.03
N	–	120	–
e	–	0.80 BSC	–
b	0.30	0.35	0.45
α	0°	–	7°

[1] All dimensions are in millimeters.

Figure 20 Mechanical Layout of the DECchip 21041



Note: All dimensions are in millimeters.

MLO-012204A

Technical Support and Ordering Information

Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

Ordering Digital Semiconductor Products

To order the DECchip 21041 PCI Ethernet LAN Controller and evaluation board, contact your local distributor.

You can order the following semiconductor products from Digital:

Product	Order Number
DECchip 21041 PCI Ethernet LAN Controller	21041–AA
DECchip 21041 Evaluation Board Kit	21A41–01
DECchip 21040 Ethernet LAN Controller for PCI	21040–AA
DECchip 21040 Evaluation Board Kit	21A40–01
DECchip 21140 PCI Fast Ethernet LAN Controller	21140–AA
DECchip 21140 Evaluation Board Kit	21A40–03

Ordering Associated Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
DECchip 21041 PCI Ethernet LAN Controller Product Brief	EC–QAWVA–TE
DECchip 21041 PCI Ethernet LAN Controller Hardware Reference Manual	EC–QAWXA–TE

Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI Local Bus Specification, Revision 2.0	PCI Special Interest Group N/S HH3–15A 5200 N.E. Elam Young Pkwy Hillsboro, OR 97124–6497 1–503–696–2000
Institute of Electrical and Electronics Engineers (IEEE) 802.3	IEEE Service Center 445 Hoes Lane P.O. Box 1331 Piscataway, NJ 08855–1331 1–800–678–IEEE (U.S. and Canada) 908–562–3805 (Outside U.S. and Canada)